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Search Results - Record(s) 1 through 10 of 11 returned.

☐ 1. Document ID: JP 07326721 A

L3: Entry 1 of 11 File: JPAB Dec 12, 1995

PUB-NO: JP407326721A
DOCUMENT-IDENTIFIER: JP 07326721 A
TITLE: SOLID IMAGE PICK-UP DEVICE

PUBN-DATE: December 12, 1995

INVENTOR-INFORMATION:
NAME
ICHINOSE, HIDEO
NOZAKI, HIDETOSHI

INT-CL (IPC): H01L 27/146; G02F 1/1343; H01L 29/41; H01L 31/0248

AB: PURPOSE: To make the low voltage driving, detection sensitivity improvement feasible by forming a steep protrusion making an avalanche amplification on the surface of a pixel electrode electrically connecting to a signal charge accumulator., CONSTITUTION: An accumulated diode 3, a signal charge leading-out gate 6 and a vertical CCD4 are formed on a semiconductor substrate 1. Next, leading- out electrodes 8 are formed on a transfer gate electrodes 6, 7 downward from the accumulated diode 3 along the periphery of an insulating film 5. Next, another insulating film 9 is formed on the leading-out electrodes 8 and the insulating film 5 so that pixel electrodes 10 may be connected to correspondingly leading-out electrodes 8 per pixel to form solid image pick-up element chips. Finally, photoconductive film 20 is formed on this solid image pick-up element chips so that hydrogenated amorphous silicon layer 22, amorphous silicon carbides 21, 23 layers may be used as the photoconductive film 20 to form a protrusion 10a for making an avalanche amplification by the photoconductive film 20, thereby enabling the low voltage driving and improving detection sensitivity., COPYRIGHT: (C)1995,JPO

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Clip Img | Image

☐ 2. Document ID: JP 05136386 A

L3: Entry 2 of 11 File: JPAB Jun 1, 1993

PUB-NO: JP405136386A
DOCUMENT-IDENTIFIER: JP 05136386 A
TITLE: IMAGE SENSOR

PUBN-DATE: June 1, 1993

INVENTOR-INFORMATION:
NAME
YAMAZAKI, KOJI

US-CL-CURRENT: 257/291; 257/292, 257/297
INT-CL (IPC): H01L 27/14; H01L 29/784; H01L 31/10; H04N 1/028

AB: PURPOSE: To reduce the dark current and the number of processes by fabricating a polycrystalline silicon film transistor using an amorphous silicon photodiode and forming at least one electrode on the amorphous silicon photodiode using polycrystalline silicon., CONSTITUTION: A photodiode 103 is of p-i-n diode structure comprising an n-type amorphous silicon carbide doped with P, intrinsic amorphous silicon and p-type amorphous silicon carbide doped with B. An ITO electrode 104 is formed on the p-type amorphous silicon carbide layer. Contrarily a thin film transistor is of MOS structure. A source 106, drain 108 and channel 107 are formed using polycrystalline silicon. A gate insulating film 109 and gate electrode 110, which are of n-type polycrystalline silicon, are formed together with n-type polycrystalline silicon layer 102. This reduces the dark current and the number of processes for forming a lower electrode., COPYRIGHT: (C)1993,JPO&Japio

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Clip. Img. | Image

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☐ 3. Document ID: JP 05003309 A

L3: Entry 3 of 11 File: JPAB Jan 8, 1993

PUB-NO: JP405003309A
DOCUMENT-IDENTIFIER: JP 05003309 A
TITLE: INSULATED GATE TYPE SEMICONDUCTOR DEVICE

PUBN-DATE: January 8, 1993

INVENTOR-INFORMATION:
NAME
MATSUKUMA, MOICHI

INT-CL (IPC): H01L 27/118; H01L 21/82

AB: PURPOSE: To realize the reduction of power consumption and high integration of insulated-gate type semiconductor device applicable to ASIC, etc., CONSTITUTION: Multi-stage element areas 10a-10d in which a source drain area 5 and gate electrode 6 are alternately formed are provided by a plurality of columns on a N well and P well. In a case where the circuit necessary for large driving power is subjected to construction, the source drain areas connected each other or the gate electrodes are connected in the area of the same type, so that a transistor having a large gate width can be constructed. The gate electrode adjacent to the transistor is connected to the power supply or grounded in order to isolate the elements. Thus, as the result that the size of the transistor becomes variable, the circuit can be constituted of appropriate transistors in size, resulting in reduction of power consumption, low heat generation and high integration., COPYRIGHT: (C)1993,JPO&Japio

4. Document ID: JP 01290266 A

L3: Entry 4 of 11 File: JPAB Nov 22, 1989

PUB-NO: JP401290266A
DOCUMENT-IDENTIFIER: JP 01290266 A
TITLE: COMPOUND SEMICONDUCTOR ELEMENT

PUBN-DATE: November 22, 1989

INVENTOR-INFORMATION:
NAME
TAKASAKI, KANETAKE

INT-CL (IPC): H01L 29/80; H01L 29/48

AB: PURPOSE: To make Schottky junction stable while holding the height of a barrier layer, by providing a p-type SiC layer between an amorphous Si-Ge-B layer and a GaAs substrate., CONSTITUTION: This element is composed of: a GaAs substrate 1 having a semi-insulation property; an n-type GaAs layer 2; an AuGe/Ni source; and drain electrodes 3 and 4 and then, a gate electrode 5 has a two-layer structure consisting of a p-type amorphous silicon carbide (a-SiC) layer 5a and an amorphous Si-Ge-B layer 5b. In other words, as Ge in amorphous Si-Ge-B is easily diffused in GaAs and forms a shallow donor level in GaAs, this element causes a depletion layer formed in SaAs by Schottky junction to be transformed into an n-type layer and then, a channel is formed. However, if a PSiC layer 5a is provided between Si-Ge-B and GaAs, diffusion of Ge in Si-Ge-B towards a GaAs side is prevented. The stability of Schottky junction is thus improved while holding the height of a barrier layer between the amorphous Si-Ge-B layer and GaAs., COPYRIGHT: (C)1989,JPO&Japio

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Clip Img | Image

5. Document ID: JP 01248667 A

L3: Entry 5 of 11 File: JPAB Oct 4, 1989

PUB-NO: JP401248667A
DOCUMENT-IDENTIFIER: JP 01248667 A
TITLE: FIELD-EFFECT TRANSISTOR

PUBN-DATE: October 4, 1989

INVENTOR-INFORMATION:
NAME
SHINOHARA, KAZUHIKO
SHINOHARA, MIKIYA
YAMANAKA, MITSUGI

US-CL-CURRENT: 257/77; 257/749
INT-CL (IPC): H01L 29/78; H01L 27/12

AB: PURPOSE: To improve ohmic contact properties with an electrode metal, and to obtain a field-effect transistor having excellent performance characteristics at high speed by forming the silicide layers of a metal on both side faces of a channel composed of a thin-film pattern having a superlattice structure., CONSTITUTION: A field-effect transistor is constituted by shaping a channel section consisting of a thin-film pattern 12 having superlattice structure in which the ultrathin films 12a of amorphous silicon hydride and the ultrathin films 12b of amorphous silicon carbide hydride are laminated alternately, source- drain electrodes 14, 15 made up of aluminum layers shaped onto both side faces of the channel section through aluminum silicide layers 13, and a gate insulating film 16 and a gate electrode 17 successively laminated to the upper layer of the thin-film pattern 12 onto a glass substrate 11. Consequently, the aluminum silicide layers 13 function as excellent ohmic contact layers, thus acquiring the field-effect transistor, operation of which is stabilized. Since a superlattice is employed as the channel section 12, the mobility of carriers is increased by 5 to 10 times as much as conventional devices, thus largely accelerating working speed., COPYRIGHT: (C)1989,JPO&Japio

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Clip Img | Image

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☐ 6. Document ID: JP 01115162 A

L3: Entry 6 of 11 File: JPAB May 8, 1989

PUB-NO: JP401115162A
DOCUMENT-IDENTIFIER: JP 01115162 A
TITLE: THIN FILM TRANSISTOR AND MANUFACTURE THEREOF

PUBN-DATE: May 8, 1989

INVENTOR-INFORMATION:
NAME
HIRAO, TAKASHI
SETSUNE, KENTARO
YOSHIDA, TETSUHISA
KAMATA, TAKESHI

US-CL-CURRENT: 257/77; 257/368, 257/632, 257/640, 257/749, 29/827
INT-CL (IPC): H01L 29/78; H01L 27/12

AB: PURPOSE: To reduce any leakage current while improving the heat resistance by a method wherein the optical forbidden band width (Eg) of an amorphous semiconductor is specified to exceed 1.9 eV i.e. Eg≥1.9 eV., CONSTITUTION: An opaque gate electrode 2 is formed and then a gate insulating film 3, an amorphous silicon carbide or amorphous silicon nitride layer 4 of Eg≥1.9 eV and a passivation insulating film 5 are successively formed on a glass substrate 1. Next, the overall surface is coated with a light sensitive resin film 6 and then the film 6 is exposed by rear side exposure process from the rear side of the glass substrate 1 to leave the same pattern as that of the gate electrode 2 for removing the passivation film 5 using the pattern as a mask. Finally, III or V group ion is implanted using the passivation film 5 as a mask to form a source.drain region. Through these procedures, any leakage current can be reduced while improving the heat resistance., COPYRIGHT: (C)1989,JPO&Japio

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Clip Img | Image

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☐ 7. Document ID: JP 63219172 A

L3: Entry 7 of 11 File: JPAB Sep 12, 1988

PUB-NO: JP363219172A
DOCUMENT-IDENTIFIER: JP 63219172 A
TITLE: THIN-FILM TRANSISTOR

PUBN-DATE: September 12, 1988

INVENTOR-INFORMATION:
NAME
AOKI, SHIGEO
UKAI, YASUHIRO

US-CL-CURRENT: 257/77; 257/57
INT-CL (IPC): H01L 29/78; H01L 27/12

AB: PURPOSE: To allow a semiconductor layer to be roughly similar to a gate insulating film in terms of thermal expansion factor and to obtain a transistor capable of excellent performance by a method wherein the semiconductor layer and the gate insulating film are both built of an amorphous silicon carbide., CONSTITUTION: A semiconductor layer 18 situated between a source electrode 12 and a drain electrode 13 is constituted of an amorphous silicon carbide a- Si1-xCx with its carbon quantity (x) not more than 0.2. On the other hand, a gate insulating film 19 is also made of an amorphous silicon carbide a-Si1-x'Cx' with its carbon quantity x' not less than the carbon quantity (x) in the semiconductor layer 18. Conductivity, which is lower when the carbon rate is higher, may be regulated within a range of 10-9∼10-16(Ωcm)-1. The semiconductor layer 18 and the gate insulating film 19 are nearly equal in terms of thermal expansion factor because they are built of similar materials, which ensures an excellent behavior., COPYRIGHT: (C)1988,JPO&Japio

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Clip Img | Image

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☐ 8. Document ID: JP 63181473 A

L3: Entry 8 of 11 File: JPAB Jul 26, 1988

PUB-NO: JP363181473A
DOCUMENT-IDENTIFIER: JP 63181473 A
TITLE: THIN-FILM TRANSISTOR

PUBN-DATE: July 26, 1988

INVENTOR-INFORMATION:
NAME
UKAI, YASUHIRO

INT-CL (IPC): H01L 29/78; H01L 27/12

AB: PURPOSE: To enhance the mobility of a field effect by a method wherein an active layer at a thin-film transistor to be used for an active liquid-display device is constituted by a heterojunction superlattice., CONSTITUTION: As an active layer 21 at a thin-film transistor which is applied to a top-gate type stagger structure, hydrogenated amorphous silicon carbide a-Si1-xCx (where x<0.5) is used for a well layer and another hydrogenated amorphous silicon carbide a-Si1-xCx (where x> 0.5) is used for a barrier layer; a multilayer laminate is constituted by laminating the two alternately. The active layer 21 is formed by a glow discharge method using silane gas SiH4 and acetylene gas C2H2. If amorphous silicon carbide a-Si1-xCx (where x > 0.5) is used for a gate insulating film 22, it is possible to form the gate insulating film 22 in succession after the formation of the active layer 21. If the amount x of carbon for amorphous silicon carbide a-Si1-xCx is more than 0.5, the conductivity in relation to the amount of carbon for amorphous silicon carbide is reduced remarkably. The mobility due to the electrical conduction of false two-dimensional carriers is increased by a quantum effect, and a big current drive force is obtained., COPYRIGHT: (C)1988,JPO&Japio

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Clip Img | Image

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☐ 9. Document ID: JP 62268167 A

L3: Entry 9 of 11 File: JPAB Nov 20, 1987

PUB-NO: JP362268167A
DOCUMENT-IDENTIFIER: JP 62268167 A
TITLE: THIN-FILM PRESSURE SENSOR

PUBN-DATE: November 20, 1987

INVENTOR-INFORMATION:
NAME
KAMAIKE, MAKOTO
TACHIKA, ATSUSHI
TANAKA, AKI

US-CL-CURRENT: 257/419
INT-CL (IPC): H01L 29/84

AB: PURPOSE: To improve adhesion by interposing a P-type amorphous silicon carbide layer between an insulating layer and an N-type semiconductor layer., CONSTITUTION: A thin-film pressure sensor is constituted of a diaphragm 1 made of stainless, an silicon oxide layer 2 as an insulating layer formed onto the surface of the diaphragm, gage sections 6 consisting of pressure-sensitive layers composed of N-type microcrystalline silicon layers 4 shaped through P-type amorphous silicon carbide layers 3 as binder layers to the upper layer of the layer 2 and electrode wiring patterns 5 made up of aluminum layers for supplying the pressure-sensitive layers with electric power, and a passivation film 7 consisting of an silicon oxide layer for coating and protecting the gage sections 6. The pressure-sensitive layer 4 for the gate section 6 is organized of four pressure-sensitive layer patterns R1∼R4, and six electrode-wiring patterns E1∼E6 for supplying these patterns R1∼R4 with electric power are shaped. Accordingly, the thin-film pressure sensor, in which a creep phenomenon is not generated and which has high reliability, is acquired., COPYRIGHT: (C)1987,JPO&Japio

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 10. Document ID: JP 62198157 A

L3: Entry 10 of 11 File: JPAB Sep 1, 1987

PUB-NO: JP362198157A
DOCUMENT-IDENTIFIER: JP 62198157 A
TITLE: THIN FILM IMAGE SENSOR

PUBN-DATE: September 1, 1987

INVENTOR-INFORMATION:
NAME
KITAGAWA, MASATOSHI
ONO, MASAHARU
HIRAO, TAKASHI

INT-CL (IPC): H01L 27/14; H04N 5/335

AB: PURPOSE: To enhance a photoelectric current and to increase an optical responding speed by providing a p-type amorphous semiconductor layer on an amorphous semiconductor layer., CONSTITUTION: A p-type amorphous semiconductor layer 14 such as a p-type amorphous silicon carbide layer (a-SiC) is formed on an amorphous semiconductor layer 13 made of an amorphous silicon (a-Si:H). For example, a source electrode 15 and a drain electrode 15 made of aluminum are formed, and an interlayer insulating layer 17 for avoiding the source, drain electrodes directly contacting with the p-type a-SiC layer is formed. A beam of light may be incident from the opposite side of a gate electrode 11 as designated by 11, or as designated by 12 when the electrode 11 is made of a transparent electrode. With this structure, the holes of electrons and holes of photocarrier generated by the light incident to the amorphous semiconductor layer are confined in the p-type layer, do not contribute to recombination to eliminate the influence of boundary level between a substrate and the amorphous semiconductor layer and the boundary level between a gate insulating layer and the amorphous semiconductor layer., COPYRIGHT: (C)1987,JPO&Japio

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Drawn Desc | Image

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Search Results - Record(s) 1 through 3 of 3 returned.

1. Document ID: US 6166401 A

L15: Entry 1 of 3 File: USPT Dec 26, 2000

US-PAT-NO: 6166401
DOCUMENT-IDENTIFIER: US 6166401 A

TITLE: Flash memory with microcrystalline silicon carbide film floating gate

DATE-ISSUED: December 26, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR	N/A	N/A

US-CL-CURRENT: 257/77

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

2. Document ID: US 6031263 A

L15: Entry 2 of 3 File: USPT Feb 29, 2000

US-PAT-NO: 6031263
DOCUMENT-IDENTIFIER: US 6031263 A

TITLE: DEAPROM and transistor with gallium nitride or gallium aluminum nitride gate

DATE-ISSUED: February 29, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR	N/A	N/A
Ahn; Kie Y.	Chappaqua	NY	N/A	N/A

US-CL-CURRENT: 257/315; 257/306, 257/318, 257/407, 438/257

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

3. Document ID: US 5886368 A

L15: Entry 3 of 3 File: USPT Mar 23, 1999

US-PAT-NO: 5886368
DOCUMENT-IDENTIFIER: US 5886368 A

TITLE: Transistor with silicon oxycarbide gate and methods of fabrication and use

DATE-ISSUED: March 23, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR	N/A	N/A
Geusic; Joseph E.	Berkeley Heights	NJ	N/A	N/A
Ahn; Kie Y.	Chappaqua	NY	N/A	N/A

US-CL-CURRENT: 257/77; 257/316, 257/412

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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ELECTRONS.USPT.	61221
AFFINITY.USPT.	58307
AFFINITIES.USPT.	5531
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☐ 1. Document ID: US 6166401 A

L14: Entry 1 of 75 File: USPT Dec 26, 2000

US-PAT-NO: 6166401
DOCUMENT-IDENTIFIER: US 6166401 A

TITLE: Flash memory with microcrystalline silicon carbide film floating gate

DATE-ISSUED: December 26, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR	N/A	N/A

US-CL-CURRENT: 257/77

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 6163485 A

L14: Entry 2 of 75 File: USPT Dec 19, 2000

US-PAT-NO: 6163485
DOCUMENT-IDENTIFIER: US 6163485 A

TITLE: Semiconductor integrated circuit data processing system

DATE-ISSUED: December 19, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kawahara; Takayuki	Higashiyamato	N/A	N/A	JPX
Sato; Hiroshi	Ome	N/A	N/A	JPX
Nozoe; Atsushi	Ome	N/A	N/A	JPX
Yoshida; Keiichi	Ome	N/A	N/A	JPX
Noda; Satoshi	Ome	N/A	N/A	JPX
Kubono; Shoji	Akishima	N/A	N/A	JPX
Kotani; Hiroaki	Ome	N/A	N/A	JPX
Kimura; Katsutaka	Akishima	N/A	N/A	JPX

US-CL-CURRENT: 365/185.24; 365/185.29

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

3. Document ID: US 6144581 A

L14: Entry 3 of 75 File: USPT Nov 7, 2000

US-PAT-NO: 6144581
DOCUMENT-IDENTIFIER: US 6144581 A

TITLE: pMOS EEPROM non-volatile data storage

DATE-ISSUED: November 7, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Diorio; Christopher J.	Torrance	CA	N/A	N/A
Mead; Carver A.	Pasadena	CA	N/A	N/A

US-CL-CURRENT: 365/185.03; 257/315, 365/185.01

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw Desc | Image

4. Document ID: US 6143636 A

L14: Entry 4 of 75 File: USPT Nov 7, 2000

US-PAT-NO: 6143636
DOCUMENT-IDENTIFIER: US 6143636 A

TITLE: High density flash memory

DATE-ISSUED: November 7, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR	N/A	N/A
Noble; Wendell P.	Milton	VT	N/A	N/A

US-CL-CURRENT: 438/587; 257/315, 257/319, 438/212, 438/259, 438/268

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw Desc | Image

5. Document ID: US 6137120 A

L14: Entry 5 of 75 File: USPT Oct 24, 2000

US-PAT-NO: 6137120
DOCUMENT-IDENTIFIER: US 6137120 A

TITLE: Semiconductor device and method of fabricating the same

DATE-ISSUED: October 24, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shindo; Masahiro	Toyonaka	N/A	N/A	JPX
Kosaka; Daisuke	Takarazuka	N/A	N/A	JPX
Hikawa; Tetsuo	Kobe	N/A	N/A	JPX
Takata; Akira	Kobe	N/A	N/A	JPX
Ukai; Yukihiro	Suita	N/A	N/A	JPX
Sawada; Takashi	Kobe	N/A	N/A	JPX
Asakawa; Toshifumi	Yamato	N/A	N/A	JPX

US-CL-CURRENT: 257/66; 257/347, 257/350, 257/57, 257/72

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 6134148 A

L14: Entry 6 of 75 File: USPT Oct 17, 2000

US-PAT-NO: 6134148
DOCUMENT-IDENTIFIER: US 6134148 A

TITLE: Semiconductor integrated circuit and data processing system

DATE-ISSUED: October 17, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kawahara; Takayuki	Higashiyamato	N/A	N/A	JPX
Sato; Hiroshi	Ome	N/A	N/A	JPX
Nozoe; Atsushi	Ome	N/A	N/A	JPX
Yoshida; Keiichi	Ome	N/A	N/A	JPX
Noda; Satoshi	Ome	N/A	N/A	JPX
Kubono; Shoji	Akishima	N/A	N/A	JPX
Kotani; Hiroaki	Ome	N/A	N/A	JPX
Kimura; Katsutaka	Akishima	N/A	N/A	JPX

US-CL-CURRENT: 365/185.28; 365/185.03

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 7. Document ID: US 6124729 A

L14: Entry 7 of 75 File: USPT Sep 26, 2000

US-PAT-NO: 6124729
DOCUMENT-IDENTIFIER: US 6124729 A

TITLE: Field programmable logic arrays with vertical transistors

DATE-ISSUED: September 26, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Noble; Wendell P.	Milton	VT	N/A	N/A
Forbes; Leonard	Corvallis	OR	N/A	N/A

US-CL-CURRENT: 326/41; 326/101, 326/44, 326/45, 326/47

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 8. Document ID: US 6125053 A

L14: Entry 8 of 75 File: USPT Sep 26, 2000

US-PAT-NO: 6125053
DOCUMENT-IDENTIFIER: US 6125053 A

TITLE: Semiconductor structure for long-term learning

DATE-ISSUED: September 26, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Diorio; Christopher J.	Torrance	CA	N/A	N/A
Mead; Carver A.	Pasadena	CA	N/A	N/A

US-CL-CURRENT: 365/185.03; 257/315, 365/185.28

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 9. Document ID: US 6122704 A

L14: Entry 9 of 75 File: USPT Sep 19, 2000

US-PAT-NO: 6122704
DOCUMENT-IDENTIFIER: US 6122704 A

TITLE: Integrated circuit for identifying an item via a serial port

DATE-ISSUED: September 19, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hass; Steven N.	Carrollton	TX	N/A	N/A
Bolan; Michael L.	Dallas	TX	N/A	N/A

US-CL-CURRENT: 711/100; 711/162, 712/1

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 10. Document ID: US 6122209 A

L14: Entry 10 of 75 File: USPT Sep 19, 2000

US-PAT-NO: 6122209
DOCUMENT-IDENTIFIER: US 6122209 A

TITLE: Method of margin testing programmable interconnect cell

DATE-ISSUED: September 19, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pass; Christopher J.	San Jose	CA	N/A	N/A
Sansbury; James D.	Portola Valley	CA	N/A	N/A
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A
Turner; John E.	Santa Cruz	CA	N/A	N/A
Patel; Rakesh H.	Cupertino	CA	N/A	N/A
Wright; Peter J.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 365/201; 365/185.05, 365/63, 365/72

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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Term	Documents
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READ.USPT.	375873
READA.USPT.	10
READAB.USPT.	3
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☐ 13. Document ID: US 6112275 A

L14: Entry 13 of 75 File: USPT Aug 29, 2000

US-PAT-NO: 6112275
DOCUMENT-IDENTIFIER: US 6112275 A

TITLE: Method of communicating over a single wire bus between a host device and a module device which measures thermal accumulation over time

DATE-ISSUED: August 29, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Curry; Stephen M.	Dallas	TX	N/A	N/A
Bolan; Michael L.	Dallas	TX	N/A	N/A
Deierling; Kevin E.	Dallas	TX	N/A	N/A
Payne, II; William Lee	Garland	TX	N/A	N/A
Kurkowski; Hal	Dallas	TX	N/A	N/A
Dias; Donald R.	Carrollton	TX	N/A	N/A
Zanders; Gary V.	Dallas	TX	N/A	N/A
Lee; Robert D.	Denton	TX	N/A	N/A
Lehmann; Guenter H.	The Colony	TX	N/A	N/A

US-CL-CURRENT: 711/100; 710/100, 710/107, 711/1, 711/4

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 14. Document ID: US 6108239 A

L14: Entry 14 of 75 File: USPT Aug 22, 2000

US-PAT-NO: 6108239
DOCUMENT-IDENTIFIER: US 6108239 A

TITLE: High-density nonvolatile memory cell

DATE-ISSUED: August 22, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sekariapuram; Seshan	Fremont	CA	N/A	N/A
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 365/185.28; 365/185.01, 365/185.18, 365/185.26

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 15. Document ID: US 6106734 A

L14: Entry 15 of 75 File: USPT Aug 22, 2000

US-PAT-NO: 6106734
DOCUMENT-IDENTIFIER: US 6106734 A

TITLE: Micromachine manufacture using gas beam crystallization

DATE-ISSUED: August 22, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shindo; Masahiro	Toyonaka	N/A	N/A	JPX
Kosaka; Daisuke	Takarazuka	N/A	N/A	JPX
Hikawa; Tetsuo	Kobe	N/A	N/A	JPX
Takata; Akira	Kobe	N/A	N/A	JPX
Ukai; Yukihiro	Suita	N/A	N/A	JPX
Sawada; Takashi	Kobe	N/A	N/A	JPX
Asakawa; Toshifumi	Yamato	N/A	N/A	JPX

US-CL-CURRENT: 216/2; 117/9, 438/52, 438/53

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 16. Document ID: US 6102962 A

L14: Entry 16 of 75 File: USPT Aug 15, 2000.

US-PAT-NO: 6102962
DOCUMENT-IDENTIFIER: US 6102962 A

TITLE: Method for estimating quiescent current in integrated circuits

DATE-ISSUED: August 15, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sugasawara; Emery O.	Pleasanton	CA	N/A	N/A
Graef; Stefan	Milpitas	CA	N/A	N/A

US-CL-CURRENT: 716/5; 716/11

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 17. Document ID: US 6097073 A

L14: Entry 17 of 75 File: USPT Aug 1, 2000

US-PAT-NO: 6097073
DOCUMENT-IDENTIFIER: US 6097073 A

TITLE: Triangular semiconductor or gate

DATE-ISSUED: August 1, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Sunnyvale	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashok K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valeriy B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata Oblast	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 257/401; 257/204, 257/776

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 18. Document ID: US 6091640 A

L14: Entry 18 of 75 File: USPT Jul 18, 2000

US-PAT-NO: 6091640
DOCUMENT-IDENTIFIER: US 6091640 A

TITLE: Semiconductor integrated circuit with multiple write operation modes

DATE-ISSUED: July 18, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kawahara; Takayuki	Higashiyamato	N/A	N/A	JPX
Sato; Hiroshi	Ome	N/A	N/A	JPX
Nozoe; Atsushi	Ome	N/A	N/A	JPX
Yoshida; Keiichi	Ome	N/A	N/A	JPX
Noda; Satoshi	Ome	N/A	N/A	JPX
Kubono; Shoji	Akishima	N/A	N/A	JPX
Kotani; Hiroaki	Ome	N/A	N/A	JPX
Kimura; Katsutaka	Akishima	N/A	N/A	JPX

US-CL-CURRENT: 365/185.28; 365/185.22

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 19. Document ID: US 6091102 A

L14: Entry 19 of 75 File: USPT Jul 18, 2000

US-PAT-NO: 6091102
DOCUMENT-IDENTIFIER: US 6091102 A

TITLE: High-density nonvolatile memory cell

DATE-ISSUED: July 18, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sekariapuram; Seshan	Fremont	CA	N/A	N/A
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 257/316; 257/317

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 20. Document ID: US 6081449 A

L14: Entry 20 of 75 File: USPT Jun 27, 2000

US-PAT-NO: 6081449
DOCUMENT-IDENTIFIER: US 6081449 A

TITLE: High-density nonvolatile memory cell

DATE-ISSUED: June 27, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sekariapuram; Seshan	Fremont	CA	N/A	N/A
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 365/185.05; 257/315, 257/316, 365/185.01

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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Generate Collection

Term	Documents
READ$	0
READ.USPT.	375873
READA.USPT.	10
READAB.USPT.	3
READABE.USPT.	2
READABI.USPT.	1
READABIE.USPT.	1
READABILITIES.USPT.	1
READABILITY.USPT.	4051
READABILITY/.USPT.	1
(L13 AND READ$ AND DATA).USPT.	75

WEST

Your wildcard search against 2000 terms has yielded the results below

Search for additional matches among the next 2000 terms

Generate Collection

Search Results - Record(s) 21 through 30 of 75 returned.

☐ 21. Document ID: US 6077745 A

L14: Entry 21 of 75 File: USPT Jun 20, 2000

US-PAT-NO: 6077745
DOCUMENT-IDENTIFIER: US 6077745 A

TITLE: Self-aligned diffused source vertical transistors with stack capacitors in a 4F-square memory cell array

DATE-ISSUED: June 20, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Burns, Jr.; Stuart Mcallister	Ridgefield	CT	N/A	N/A
Hanafi; Hussein Ibrahim	Goldens Bridge	NY	N/A	N/A
Welser; Jeffrey J.	Greenwich	CT	N/A	N/A
Kocon; Waldemar Walter	Wappingers Fall	NY	N/A	N/A
Kalter; Howard Leo	Colchester	VT	N/A	N/A

US-CL-CURRENT: 438/270; 438/207, 438/268, 438/294, 438/299, 438/300

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 22. Document ID: US 6078521 A

L14: Entry 22 of 75 File: USPT Jun 20, 2000

US-PAT-NO: 6078521
DOCUMENT-IDENTIFIER: US 6078521 A

TITLE: Nonvolatile configuration cells and cell arrays

DATE-ISSUED: June 20, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A
Sansbury; James D.	Portola Valley	CA	N/A	N/A

US-CL-CURRENT: 365/185.18; 365/185.24, 365/185.28

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 23. Document ID: US 6052309 A

L14: Entry 23 of 75 File: USPT Apr 18, 2000

US-PAT-NO: 6052309
DOCUMENT-IDENTIFIER: US 6052309 A

TITLE: Nonvolatile configuration cells and cell arrays

DATE-ISSUED: April 18, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A
Sansbury; James D.	Portola Valley	CA	N/A	N/A

US-CL-CURRENT: 365/185.28; 365/185.1

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 24. Document ID: US 6040210 A

L14: Entry 24 of 75 File: USPT Mar 21, 2000

US-PAT-NO: 6040210
DOCUMENT-IDENTIFIER: US 6040210 A

TITLE: 2F-square memory cell for gigabit memory applications

DATE-ISSUED: March 21, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Burns, Jr.; Stuart Mcallister	Ridgefield	CT	N/A	N/A
Hanafi; Hussein Ibrahim	Goldens Bridge	NY	N/A	N/A

US-CL-CURRENT: 438/238; 438/242, 438/245, 438/263, 438/266, 438/270

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 25. Document ID: US 6036101 A

L14: Entry 25 of 75 File: USPT Mar 14, 2000

US-PAT-NO: 6036101
DOCUMENT-IDENTIFIER: US 6036101 A

TITLE: Electronic labeling systems and methods and electronic card systems and methods

DATE-ISSUED: March 14, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hass; Steven N.	Carrollton	TX	N/A	N/A
Bolan; Michael L.	Dallas	TX	N/A	N/A

US-CL-CURRENT: 235/492; 235/439, 235/441

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 26. Document ID: US 6034389 A

L14: Entry 26 of 75 File: USPT Mar 7, 2000

US-PAT-NO: 6034389
DOCUMENT-IDENTIFIER: US 6034389 A

TITLE: Self-aligned diffused source vertical transistors with deep trench capacitors in a 4F-square memory cell array

DATE-ISSUED: March 7, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Burns, Jr.; Stuart Mcallister	Ridgefield	CT	N/A	N/A
Hanafi; Hussein Ibrahim	Goldens Bridge	NY	N/A	N/A
Kalter; Howard Leo	Colchester	VT	N/A	N/A
Welser; Jeffrey J.	Greenwich	CT	N/A	N/A
Kocon; Waldemar Walter	Wappingers Falls	NY	N/A	N/A

US-CL-CURRENT: 257/301; 257/906, 257/908, 438/242, 438/243, 438/427

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 27. Document ID: US 6033957 A

L14: Entry 27 of 75 File: USPT Mar 7, 2000

US-PAT-NO: 6033957
DOCUMENT-IDENTIFIER: US 6033957 A

TITLE: 4F-square memory cell having vertical floating-gate transistors with self-aligned shallow trench isolation

DATE-ISSUED: March 7, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Burns, Jr.; Stuart Mcallister	Ridgefield	CT	N/A	N/A
Hanafi; Hussein Ibrahim	Goldens Bridge	NY	N/A	N/A
Welser; Jeffrey J.	Greenwich	CT	N/A	N/A
Kocon; Waldemar Walter	Wappingers Fall	NY	N/A	N/A

US-CL-CURRENT: 438/270; 438/207, 438/268, 438/283, 438/284, 438/294, 438/299, 438/300

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 28. Document ID: US 6031263 A

L14: Entry 28 of 75 File: USPT Feb 29, 2000

US-PAT-NO: 6031263
DOCUMENT-IDENTIFIER: US 6031263 A

TITLE: DEAPROM and transistor with gallium nitride or gallium aluminum nitride gate

DATE-ISSUED: February 29, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR	N/A	N/A
Ahn; Kie Y.	Chappaqua	NY	N/A	N/A

US-CL-CURRENT: 257/315; 257/306, 257/318, 257/407, 438/257

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 29. Document ID: US 6028787 A

L14: Entry 29 of 75 File: USPT Feb 22, 2000

US-PAT-NO: 6028787
DOCUMENT-IDENTIFIER: US 6028787 A

TITLE: Nonvolatile static memory circuit

DATE-ISSUED: February 22, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sansbury; James D.	Portola Valley	CA	N/A	N/A
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 365/185.01; 365/154, 365/156, 365/185.07, 365/185.08

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 30. Document ID: US 6025252 A

L14: Entry 30 of 75 File: USPT Feb 15, 2000

US-PAT-NO: 6025252
DOCUMENT-IDENTIFIER: US 6025252 A

TITLE: Semiconductor device and method of fabricating the same

DATE-ISSUED: February 15, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shindo; Masahiro	Toyonaka	N/A	N/A	JPX
Kosaka; Daisuke	Takarazuka	N/A	N/A	JPX
Hikawa; Tetsuo	Kobe	N/A	N/A	JPX
Takata; Akira	Kobe	N/A	N/A	JPX
Ukai; Yukihiro	Suita	N/A	N/A	JPX
Sawada; Takashi	Kobe	N/A	N/A	JPX
Asakawa; Toshifumi	Yamato	N/A	N/A	JPX

US-CL-CURRENT: 438/509; 136/249, 136/260, 136/262, 438/503

Generate Collection

Term	Documents
READ$	0
READ.USPT.	375873
READA.USPT.	10
READAB.USPT.	3
READABE.USPT.	2
READABI.USPT.	1
READABIE.USPT.	1
READABILITIES.USPT.	1
READABILITY.USPT.	4051
READABILITY/.USPT.	1
(L13 AND READ$ AND DATA).USPT.	75

There are more results than shown above. Click here to view the entire set.

Display 10 Documents, starting with Document: 31

Display Format: CIT Change Format

WEST

Your wildcard search against 2000 terms has yielded the results below

Search for additional matches among the next 2000 terms

Generate Collection

Search Results - Record(s) 31 through 40 of 75 returned.

☐ 31. Document ID: US 6018476 A

L14: Entry 31 of 75 File: USPT Jan 25, 2000

US-PAT-NO: 6018476
DOCUMENT-IDENTIFIER: US 6018476 A

TITLE: Nonvolatile configuration cells and cell arrays

DATE-ISSUED: January 25, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A
Sansbury; James D.	Portola Valley	CA	N/A	N/A

US-CL-CURRENT: 365/185.23; 365/185.25, 365/185.28

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 32. Document ID: US 6016255 A

L14: Entry 32 of 75 File: USPT Jan 18, 2000

US-PAT-NO: 6016255
DOCUMENT-IDENTIFIER: US 6016255 A

TITLE: Portable data carrier mounting system

DATE-ISSUED: January 18, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bolan; Michael L.	Dallas	TX	N/A	N/A
Fekete; Nicholas M. G.	Richardson	TX	N/A	N/A

US-CL-CURRENT: 361/807; 361/809

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 33. Document ID: US 6013548 A

L14: Entry 33 of 75 File: USPT Jan 11, 2000

US-PAT-NO: 6013548
DOCUMENT-IDENTIFIER: US 6013548 A

TITLE: Self-aligned diffused source vertical transistors with deep trench capacitors in a 4F-square memory cell array

DATE-ISSUED: January 11, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Burns, Jr.; Stuart Mcallister	Ridgefield	CT	N/A	N/A
Hanafi; Hussein Ibrahim	Goldens Bridge	NY	N/A	N/A
Kalter; Howard Leo	Colchester	VT	N/A	N/A
Welser; Jeffrey J.	Greenwich	CT	N/A	N/A
Kocon; Waldemar Walter	Wappingers Falls	NY	N/A	N/A

US-CL-CURRENT: 438/242; 438/243, 438/427

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 34. Document ID: US 6005806 A

L14: Entry 34 of 75 File: USPT Dec 21, 1999

US-PAT-NO: 6005806
DOCUMENT-IDENTIFIER: US 6005806 A

TITLE: Nonvolatile configuration cells and cell arrays

DATE-ISSUED: December 21, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A
Sansbury; James D.	Portola Valley	CA	N/A	N/A

US-CL-CURRENT: 365/185.23; 365/185.05

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 35. Document ID: US 5998263 A

L14: Entry 35 of 75 File: USPT Dec 7, 1999

US-PAT-NO: 5998263
DOCUMENT-IDENTIFIER: US 5998263 A

TITLE: High-density nonvolatile memory cell

DATE-ISSUED: December 7, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sekariapuram; Seshan	Fremont	CA	N/A	N/A
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 438/259; 438/561, 438/700

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 36. Document ID: US 5990509 A

L14: Entry 36 of 75 File: USPT Nov 23, 1999

US-PAT-NO: 5990509
DOCUMENT-IDENTIFIER: US 5990509 A

TITLE: 2F-square memory cell for gigabit memory applications

DATE-ISSUED: November 23, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Burns, Jr.; Stuart Mcallister	Ridgefield	CT	N/A	N/A
Hanafi; Hussein Jbrahim	Goldens Bridge	NY	N/A	N/A
Welser; Jeffrey J.	Greenwich	CT	N/A	N/A

US-CL-CURRENT: 257/296; 257/316, 257/330, 257/623, 438/257

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 37. Document ID: US 5991225 A

L14: Entry 37 of 75 File: USPT Nov 23, 1999

US-PAT-NO: 5991225
DOCUMENT-IDENTIFIER: US 5991225 A

TITLE: Programmable memory address decode array with vertical transistors

DATE-ISSUED: November 23, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR	N/A	N/A
Noble; Wendell P.	Milton	VT	N/A	N/A

US-CL-CURRENT: 365/230.06; 365/230.02

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 38. Document ID: US 5973356 A

L14: Entry 38 of 75 File: USPT Oct 26, 1999

US-PAT-NO: 5973356
DOCUMENT-IDENTIFIER: US 5973356 A

TITLE: Ultra high density flash memory

DATE-ISSUED: October 26, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Noble; Wendell P.	Milton	VT	N/A	N/A
Forbes; Leonard	Corvallis	OR	N/A	N/A

US-CL-CURRENT: 257/319; 257/314, 257/315, 257/316, 365/185.01, 365/185.26

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 39. Document ID: US 5973376 A

L14: Entry 39 of 75 File: USPT Oct 26, 1999

US-PAT-NO: 5973376
DOCUMENT-IDENTIFIER: US 5973376 A

TITLE: Architecture having diamond shaped or parallelogram shaped cells

DATE-ISSUED: October 26, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Sunnyvale	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashok K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valeriy B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata Oblast	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 257/401; 257/204, 257/207, 257/211, 257/776

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 40. Document ID: US 5959885 A

L14: Entry 40 of 75 File: USPT Sep 28, 1999

US-PAT-NO: 5959885
DOCUMENT-IDENTIFIER: US 5959885 A

TITLE: Non-volatile memory array using single poly EEPROM in standard CMOS process

DATE-ISSUED: September 28, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rao; Kameswara K.	San Jose	CA	N/A	N/A

US-CL-CURRENT: 365/185.07; 365/226

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

Generate Collection

Term	Documents
READ$	0
READ.USPT.	375873
READA.USPT.	10
READAB.USPT.	3
READABE.USPT.	2
READABI.USPT.	1
READABIE.USPT.	1
READABILITIES.USPT.	1
READABILITY.USPT.	4051
READABILITY/.USPT.	1
(L13 AND READ$ AND DATA).USPT.	75

There are more results than shown above. Click here to view the entire set.

Display 10 Documents, starting with Document: 41

Display Format: CIT Change Format

WEST

Your wildcard search against 2000 terms has yielded the results below

Search for additional matches among the next 2000 terms

Generate Collection

Search Results - Record(s) 41 through 50 of 75 returned.

☐ 41. Document ID: US 5949712 A

L14: Entry 41 of 75 File: USPT Sep 7, 1999

US-PAT-NO: 5949712
DOCUMENT-IDENTIFIER: US 5949712 A

TITLE: Non-volatile memory array using gate breakdown structure

DATE-ISSUED: September 7, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rao; Kameswara K.	San Jose	CA	N/A	N/A
Voogel; Martin L.	Santa Clara	CA	N/A	N/A

US-CL-CURRENT: 365/185.07; 365/226

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 42. Document ID: US 5949710 A

L14: Entry 42 of 75 File: USPT Sep 7, 1999

US-PAT-NO: 5949710
DOCUMENT-IDENTIFIER: US 5949710 A

TITLE: Programmable interconnect junction

DATE-ISSUED: September 7, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pass; Christopher J.	San Jose	CA	N/A	N/A
Sansbury; James D.	Portola Valley	CA	N/A	N/A
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A
Turner; John E.	Santa Cruz	CA	N/A	N/A
Patel; Rakesh H.	Cupertino	CA	N/A	N/A
Wright; Peter J.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 365/185.05; 365/185.28, 365/63, 365/72

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 43. Document ID: US 5943267 A

L14: Entry 43 of 75 File: USPT Aug 24, 1999

US-PAT-NO: 5943267
DOCUMENT-IDENTIFIER: US 5943267 A

TITLE: High-density nonvolatile memory cell

DATE-ISSUED: August 24, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sekariapuram; Seshan	Fremont	CA	N/A	N/A
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 365/185.28; 365/185.14, 365/185.24, 365/185.26

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 44. Document ID: US 5929477 A

L14: Entry 44 of 75 File: USPT Jul 27, 1999

US-PAT-NO: 5929477
DOCUMENT-IDENTIFIER: US 5929477 A

TITLE: Self-aligned diffused source vertical transistors with stack capacitors in a 4F-square memory cell array

DATE-ISSUED: July 27, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
McAllister Burns, Jr.; Stuart	Ridgefield	CT	N/A	N/A
Hanafi; Hussein Ibrahim	Goldens Bridge	NY	N/A	N/A
Welser; Jeffrey J.	Greenwich	CT	N/A	N/A
Kocon; Waldemar Walter	Wappingers Fall	NY	N/A	N/A
Kalter; Howard Leo	Colchester	VT	N/A	N/A

US-CL-CURRENT: 257/306; 257/296, 257/302, 257/303, 438/248, 438/386, 438/396

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 45. Document ID: US 5898613 A

L14: Entry 45 of 75 File: USPT Apr 27, 1999

US-PAT-NO: 5898613
DOCUMENT-IDENTIFIER: US 5898613 A

TITLE: pMOS analog EEPROM cell

DATE-ISSUED: April 27, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Diorio; Christopher J.	Torrance	CA	N/A	N/A
Mead; Carver A.	Pasadena	CA	N/A	N/A

US-CL-CURRENT: 365/185.03; 257/315, 365/185.18, 365/185.28

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 46. Document ID: US 5889329 A

L14: Entry 46 of 75 File: USPT Mar 30, 1999

US-PAT-NO: 5889329
DOCUMENT-IDENTIFIER: US 5889329 A

TITLE: Tri-directional interconnect architecture for SRAM

DATE-ISSUED: March 30, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Sunnyvale	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashok K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valeriv B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata Oblast	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 257/758; 257/206, 257/211, 257/401, 257/776

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 47. Document ID: US 5886368 A

L14: Entry 47 of 75 File: USPT Mar 23, 1999

US-PAT-NO: 5886368
DOCUMENT-IDENTIFIER: US 5886368 A

TITLE: Transistor with silicon oxycarbide gate and methods of fabrication and use

DATE-ISSUED: March 23, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR	N/A	N/A
Geusic; Joseph E.	Berkeley Heights	NJ	N/A	N/A
Ahn; Kie Y.	Chappaqua	NY	N/A	N/A

US-CL-CURRENT: 257/77; 257/316, 257/412

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 48. Document ID: US 5874760 A

L14: Entry 48 of 75 File: USPT Feb 23, 1999

US-PAT-NO: 5874760
DOCUMENT-IDENTIFIER: US 5874760 A

TITLE: 4F-square memory cell having vertical floating-gate transistors with self-aligned shallow trench isolation

DATE-ISSUED: February 23, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Burns, Jr.; Stuart Mcallister	Ridgefield	CT	N/A	N/A
Hanafi; Hussein Ibrahim	Goldens Bridge	NY	N/A	N/A
Welser; Jeffrey J.	Greenwich	CT	N/A	N/A
Kocon; Waldemar Walter	Wappingers Fall	NY	N/A	N/A

US-CL-CURRENT: 257/315; 257/318

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 49. Document ID: US 5872380 A

L14: Entry 49 of 75 File: USPT Feb 16, 1999

US-PAT-NO: 5872380
DOCUMENT-IDENTIFIER: US 5872380 A

TITLE: Hexagonal sense cell architecture

DATE-ISSUED: February 16, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Sunnyvale	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashok K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valerity B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 257/369; 257/206, 257/368, 257/371, 257/391, 326/38, 327/563

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 50. Document ID: US 5864165 A

L14: Entry 50 of 75 File: USPT Jan 26, 1999

US-PAT-NO: 5864165
DOCUMENT-IDENTIFIER: US 5864165 A

TITLE: Triangular semiconductor NAND gate

DATE-ISSUED: January 26, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Sunnyvale	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashok K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valeriy B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata Oblast	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 257/401; 257/204, 257/206, 257/211

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 51. Document ID: US 5862091 A

L14: Entry 51 of 75 File: USPT Jan 19, 1999

US-PAT-NO: 5862091
DOCUMENT-IDENTIFIER: US 5862091 A

TITLE: Memory accessible in read mode only

DATE-ISSUED: January 19, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bion; Thierry	Fontaine	N/A	N/A	FRX
Ferrant; Richard	Berkeley	CA	N/A	N/A

US-CL-CURRENT: 365/207; 365/104, 365/208

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 52. Document ID: US 5835402 A

L14: Entry 52 of 75 File: USPT Nov 10, 1998

US-PAT-NO: 5835402
DOCUMENT-IDENTIFIER: US 5835402 A

TITLE: Non-volatile storage for standard CMOS integrated circuits

DATE-ISSUED: November 10, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rao; Kameswara K.	San Jose	CA	N/A	N/A
Voogel; Martin L.	Santa Clara	CA	N/A	N/A

US-CL-CURRENT: 365/149; 365/102, 365/103, 365/185.07

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 53. Document ID: US 5834821 A

L14: Entry 53 of 75 File: USPT Nov 10, 1998

US-PAT-NO: 5834821
DOCUMENT-IDENTIFIER: US 5834821 A

TITLE: Triangular semiconductor "AND" gate device

DATE-ISSUED: November 10, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Sunnyvale	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashok K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valeriy B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata Oblast	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 257/401; 257/204, 257/208, 257/365

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 54. Document ID: US 5822214 A

L14: Entry 54 of 75 File: USPT Oct 13, 1998

US-PAT-NO: 5822214
DOCUMENT-IDENTIFIER: US 5822214 A

TITLE: CAD for hexagonal architecture

DATE-ISSUED: October 13, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Los Altos Hill	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashok K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valeriv B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 716/10; 716/11, 716/19

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 55. Document ID: US 5812450 A

L14: Entry 55 of 75 File: USPT Sep 22, 1998

US-PAT-NO: 5812450
DOCUMENT-IDENTIFIER: US 5812450 A

TITLE: Nonvolatile SRAM cells and cell arrays

DATE-ISSUED: September 22, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sansbury; James D.	Portola Valley	CA	N/A	N/A
Madurawe; Raminda U.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 365/185.01; 365/104, 365/154, 365/185.07, 365/185.08, 365/94

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 56. Document ID: US 5811863 A

L14: Entry 56 of 75 File: USPT Sep 22, 1998

US-PAT-NO: 5811863
DOCUMENT-IDENTIFIER: US 5811863 A

TITLE: Transistors having dynamically adjustable characteristics

DATE-ISSUED: September 22, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Sunnyvale	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashook K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valeriy B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata Oblast	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 257/401; 257/204, 257/288, 257/331, 257/365

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 57. Document ID: US 5808330 A

L14: Entry 57 of 75 File: USPT Sep 15, 1998

US-PAT-NO: 5808330
DOCUMENT-IDENTIFIER: US 5808330 A

TITLE: Polydirectional non-orthoginal three layer interconnect architecture

DATE-ISSUED: September 15, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Sunnyvale	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashok K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valeriv B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata Oblast	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 257/208; 257/204, 257/207, 257/211, 257/758, 438/128

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 58. Document ID: US 5801422 A

L14: Entry 58 of 75 File: USPT Sep 1, 1998

US-PAT-NO: 5801422
DOCUMENT-IDENTIFIER: US 5801422 A

TITLE: Hexagonal SRAM architecture

DATE-ISSUED: September 1, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Sunnyvale	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashok K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valeriy B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata Oblast	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 257/369; 257/204, 257/401

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 59. Document ID: US 5789770 A

L14: Entry 59 of 75 File: USPT Aug 4, 1998

US-PAT-NO: 5789770
DOCUMENT-IDENTIFIER: US 5789770 A

TITLE: Hexagonal architecture with triangular shaped cells

DATE-ISSUED: August 4, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Los Altos Hills	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashok K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valeriv B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata Oblast	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 257/206; 257/204, 257/365, 257/401

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 60. Document ID: US 5777360 A

L14: Entry 60 of 75 File: USPT Jul 7, 1998

US-PAT-NO: 5777360
DOCUMENT-IDENTIFIER: US 5777360 A

TITLE: Hexagonal field programmable gate array architecture

DATE-ISSUED: July 7, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rostoker; Michael D.	Boulder Creek	CA	N/A	N/A
Koford; James S.	Mountain View	CA	N/A	N/A
Scepanovic; Ranko	San Jose	CA	N/A	N/A
Jones; Edwin R.	Sunnyvale	CA	N/A	N/A
Padmanahben; Gobi R.	Sunnyvale	CA	N/A	N/A
Kapoor; Ashok K.	Palo Alto	CA	N/A	N/A
Kudryavtsev; Valeriy B.	Moscow	N/A	N/A	RUX
Andreev; Alexander E.	Moskovskata Oblast	N/A	N/A	RUX
Aleshin; Stanislav V.	Moscow	N/A	N/A	RUX
Podkolzin; Alexander S.	Moscow	N/A	N/A	RUX

US-CL-CURRENT: 257/315; 257/401, 257/529, 257/665

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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L3: Entry 8 of 11 File: JPAB Jul 26, 1988

PUB-NO: JP363181473A
DOCUMENT-IDENTIFIER: JP 63181473 A
TITLE: THIN-FILM TRANSISTOR

PUBN-DATE: July 26, 1988

INVENTOR-INFORMATION:
NAME
UKAI, YASUHIRO

ASSIGNEE-INFORMATION:
NAME COUNTRY
HOSIDEN ELECTRONICS CO LTD N/A

APPL-NO: JP62013786
APPL-DATE: January 23, 1987

INT-CL (IPC): H01L 29/78; H01L 27/12

ABSTRACT:

PURPOSE: To enhance the mobility of a field effect by a method wherein an active layer at a thin-film transistor to be used for an active liquid-display device is constituted by a heterojunction superlattice.

CONSTITUTION: As an active layer 21 at a thin-film transistor which is applied to a top-gate type stagger structure, hydrogenated amorphous silicon carbide a-Si1-xCx (where x<0.5) is used for a well layer and another hydrogenated amorphous silicon carbide a-Si1-xCx (where x> 0.5) is used for a barrier layer; a multilayer laminate is constituted by laminating the two alternately. The active layer 21 is formed by a glow discharge method using silane gas SiH4 and acetylene gas C2H2. If amorphous silicon carbide a-Si1-xCx (where x > 0.5) is used for a gate insulating film 22, it is possible to form the gate insulating film 22 in succession after the formation of the active layer 21. If the amount x of carbon for amorphous silicon carbide a-Si1-xCx is more than 0.5, the conductivity in relation to the amount of carbon for amorphous silicon carbide is reduced remarkably. The mobility due to the electrical conduction of false two-dimensional carriers is increased by a quantum effect, and a big current drive force is obtained.

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L3: Entry 6 of 11 File: JPAB May 8, 1989

PUB-NO: JP401115162A
DOCUMENT-IDENTIFIER: JP 01115162 A
TITLE: THIN FILM TRANSISTOR AND MANUFACTURE THEREOF

PUBN-DATE: May 8, 1989

INVENTOR-INFORMATION:
NAME
HIRAO, TAKASHI
SETSUNE, KENTARO
YOSHIDA, TETSUHISA
KAMATA, TAKESHI

ASSIGNEE-INFORMATION:
NAME COUNTRY
MATSUSHITA ELECTRIC IND CO LTD N/A

APPL-NO: JP62271865
APPL-DATE: October 29, 1987

US-CL-CURRENT: 257/77; 257/368, 257/632, 257/640, 257/749, 29/827
INT-CL (IPC): H01L 29/78; H01L 27/12

ABSTRACT:

PURPOSE: To reduce any leakage current while improving the heat resistance by a method wherein the optical forbidden band width (Eg) of an amorphous semiconductor is specified to exceed 1.9 eV i.e. Eg≥1.9 eV.

CONSTITUTION: An opaque gate electrode 2 is formed and then a gate insulating film 3, an amorphous silicon carbide or amorphous silicon nitride layer 4 of Eg≥1.9 eV and a passivation insulating film 5 are successively formed on a glass substrate 1. Next, the overall surface is coated with a light sensitive resin film 6 and then the film 6 is exposed by rear side exposure process from the rear side of the glass substrate 1 to leave the same pattern as that of the gate electrode 2 for removing the passivation film 5 using the pattern as a mask. Finally, III or V group ion is implanted using the passivation film 5 as a mask to form a source.drain region. Through these procedures, any leakage current can be reduced while improving the heat resistance.

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L3: Entry 7 of 11 File: JPAB Sep 12, 1988

PUB-NO: JP363219172A
DOCUMENT-IDENTIFIER: JP 63219172 A
TITLE: THIN-FILM TRANSISTOR

PUBN-DATE: September 12, 1988

INVENTOR-INFORMATION:
NAME
AOKI, SHIGEO
UKAI, YASUHIRO

ASSIGNEE-INFORMATION:

NAME	COUNTRY
HOSIDEN ELECTRONICS CO LTD	N/A

APPL-NO: JP62052418
APPL-DATE: March 6, 1987

US-CL-CURRENT: 257/77; 257/57
INT-CL (IPC): H01L 29/78; H01L 27/12

ABSTRACT:

PURPOSE: To allow a semiconductor layer to be roughly similar to a gate insulating film in terms of thermal expansion factor and to obtain a transistor capable of excellent performance by a method wherein the semiconductor layer and the gate insulating film are both built of an amorphous silicon carbide.

CONSTITUTION: A semiconductor layer 18 situated between a source electrode 12 and a drain electrode 13 is constituted of an amorphous silicon carbide a-Si1-xCx with its carbon quantity (x) not more than 0.2. On the other hand, a gate insulating film 19 is also made of an amorphous silicon carbide a-Si1-x'Cx' with its carbon quantity x' not less than the carbon quantity (x) in the semiconductor layer 18. Conductivity, which is lower when the carbon rate is higher, may be regulated within a range of 10-9∼10-16(Ωcm)-1. The semiconductor layer 18 and the gate insulating film 19 are nearly equal in terms of thermal expansion factor because they are built of similar materials, which ensures an excellent behavior.

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L3: Entry 11 of 11 File: JPAB Jun 3, 1987

PUB-NO: JP362122275A
DOCUMENT-IDENTIFIER: JP 62122275 A
TITLE: MIS TYPE SEMICONDUCTOR DEVICE

PUBN-DATE: June 3, 1987

INVENTOR-INFORMATION:
NAME
YAMAMOTO, HIDEKAZU
ASAI, SOTOHISA
IWADE, SHUHEI
YUYA, NAOKI

ASSIGNEE-INFORMATION:
NAME COUNTRY
MITSUBISHI ELECTRIC CORP N/A

APPL-NO: JP60262749
APPL-DATE: November 22, 1985

US-CL-CURRENT: 257/66; 257/77
INT-CL (IPC): H01L 29/78; H01L 27/12

ABSTRACT:

PURPOSE: To eliminate the effect of an interface level and to obtain a highly reliable semiconductor device, by changing the composition of amorphous semiconductors, and providing the minimum value of a forbidden band at a part inner than the interface between an insulating film and the semiconductor.

CONSTITUTION: On an insulating substrate 5, a gate electrode 6 is formed. A gate insulating film 1, amorphous semiconductors, e.g., amorphous silicon carbide layers 2 and 4, and an amorphous silicon layer 3 are formed in the same film growing tank. Thereafter, source and drain electrodes 7 and 8 are formed. By forming the amorphous semiconductors having the different forbidden bands at the interface between the insulating film and the semiconductors, a potential well is formed. Since carrier charge is present in this well, the effect of the interface level is not received. In the MIS type FET having such a structure, a current path is formed as shown by an arrow, and the effect of the interface level is not exerted, too.

AB: PURPOSE: To eliminate the effect of an interface level and to obtain a highly reliable semiconductor device, by changing the composition of amorphous semiconductors, and providing the minimum value of a forbidden band at a part inner than the interface between an insulating film and the semiconductor., CONSTITUTION: On an insulating substrate 5, a gate electrode 6 is formed. A gate insulating film 1, amorphous semiconductors, e.g., amorphous silicon carbide layers 2 and 4, and an amorphous silicon layer 3 are formed in the same film growing tank. Thereafter, source and drain electrodes 7 and 8 are formed. By forming the amorphous semiconductors having the different forbidden bands at the interface between the insulating film and the semiconductors, a potential well is formed. Since carrier charge is present in this well, the effect of the interface level is not received. In the MIS type FET having such a structure, a current path is formed as shown by an arrow, and the effect of the interface level is not exerted, too.,

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USPT	l9 and source and drain	90	L10
USPT	l8 and layer	92	L9
USPT	l7 and substrate	103	L8
USPT	l6 and floating adj1 gate	114	L7
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JPAB	l2 and gate	11	L3
JPAB	l1 and (insulat$ or dielectric)	100	L2
JPAB	(amorphous adj1 silicon adj1 carbide or a-SiC or aSiC)	1154	L1